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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/964,484 | 09/28/2001 | Toru Ishida | H-1013 | 2783 |

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| EXAMINER |
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| ART UNIT | PAPER NUMBER |
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| 2826 | 5 |

DATE MAILED: 11/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/964,484 | Applicant(s) ISHIDA ET AL. | |
|---|---|---|---|
| | Examiner Alexander O Williams | Art Unit 2826 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 09/964484 Attorney's Docket #: H-1013
Filing Date: 9/28/01;

Applicant: Ishida et al.

Examiner: Alexander Williams

Applicant's election of Species (claims 1 to 24) in Paper # 4, filed 9/23/02, has been acknowledged. All claims will be examined.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 31 are rejected under 35 U.S.C. § 102(e) as being anticipated by Choi et al. (U.S. Patent Application # 2002/0084519).

1. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having on one main surface thereof a control circuit, a first bonding pad (inherit), and a plurality of second bonding pads (inherit); a second semiconductor chip **12b** having on one main surface thereof a memory circuit and a third bonding pad (inherit) and disposed on the one main surface of the first semiconductor chip, the memory circuit being controlled in accordance with a control signal generated in the control circuit on the first semiconductor chip; a first lead **11b** having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of second leads **11b** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a first bonding wire **14a** for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead; a plurality of second bonding wires **14b** for connecting the plural second bonding pads on the first semiconductor chip with the inner lead portions of the plural second leads; a third bonding wire **14b** for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead; and a resin seal member **15** for sealing the first and second semiconductor chips, the first, second and third bonding wires, and the inner lead portions of the first and second leads, wherein the control signal generated in the control circuit is outputted from the first bonding pad on the first semiconductor chip and is inputted to the third bonding pad on the semiconductor chip through the first bonding wire, the first lead and the third bonding wire.

2. A semiconductor device according to claim 1, Choi et al.'s second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

3. A semiconductor device according to claim 1, Choi et al. show an another main surface opposed of the second semiconductor chip opposed to the one main surface

thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.
4. A semiconductor device according to claim 1, Choi et al.'s first and third bonding wires are connected to one and same surface of the first lead.
5. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having on one main surface thereof a processor unit adapted to operate in accordance with a program and a plurality of bonding pads (inherit); a second semiconductor chip **12b** having on one main surface thereof a non-volatile memory unit into which are written serial data by operation of the first semiconductor chip and also having a plurality of bonding pads (inherit), the second semiconductor chip being disposed on one main surface of the first semiconductor chip; a plurality of leads **11** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; and a resin seal member **15** for sealing the first and second semiconductor chips and the inner lead portions of the plural leads, wherein the plural bonding pads on the first and second semiconductor chips are electrically connected to the inner lead portions of the plural leads.
6. A semiconductor device according to claim 5, Choi et al.'s first semiconductor chip is a chip for a microcomputer, and wherein the second semiconductor chip is a chip for an EEPROM.
7. A semiconductor device according to claim 5, Choi et al.'s plural bonding pads on the first semiconductor chip include a first bonding pad, wherein the plural bonding pads on the second semiconductor chip include a second bonding pad, wherein the first bonding pad is electrically connected to an inner lead portion of one of the plural leads through a first bonding wire, wherein the second bonding pad is electrically connected to an inner lead portion of one of the plural leads through a second bonding wire, and wherein the serial data are outputted from the first bonding pad and inputted to the second bonding pad through the first bonding wire, one of the plural leads, and the second bonding wire.
8. A semiconductor device according to claim 5, Choi et al.'s second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.
9. A semiconductor device according to claim 5, Choi et al. show wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.

10. A semiconductor device according to claim 6, Choi et al. show wherein the first and second bonding wires are connected to one and same surface of one of the plural leads.

11. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having on one main surface thereof a first bonding pad (inherit) and a plurality of second bonding pads (inherit); a second semiconductor chip **12b** having on one main surface thereof a plurality of third bonding pads (inherit) interconnected electrically, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip; a first lead **11** having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of second leads **11** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a first bonding wire for connecting the first bonding pad on the first semiconductor chip with the inner lead of the first lead; a plurality of second bonding wires (inherit) for connecting the plural second bonding pads on the first semiconductor chip with the inner lead portions of the plural second leads; a third bonding wire **14b** for connecting one of the plural third bonding pads (inherit) on the second semiconductor chip with the inner lead portion of the first lead; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portions of the first, second and third leads, and the first, second and third bonding wires.

12. A semiconductor device according to claim 11, Choi et al. show wherein the second semiconductor chip is formed in a quadrangular shape in plan, and wherein the plural third bonding pads are arranged along at least one side of the second semiconductor chip.

13. A semiconductor device according to claim 11, Choi et al. show wherein the second semiconductor chip is formed in a quadrangular shape in plan, and wherein the plural third bonding pads are arranged along at least two sides contiguous to each other of the second semiconductor chip.

14. A semiconductor device according to claim 11, Choi et al. show wherein the first bonding pad and the plural third bonding pads are bonding pads for signal.

15. A semiconductor device according to claim 11, Choi et al. show wherein the second semiconductor chip is formed in a plane size smaller than that of the first semiconductor chip.

16. A semiconductor device according to claim 11, Choi et al. show wherein another main surface of the second semiconductor chip opposed to the one main surface thereof is disposed on the one main surface of the first semiconductor chip in an opposed relation to the one main surface of the first semiconductor chip.
17. A semiconductor device according to claim 11, Choi et al. show wherein the first and third bonding wires are connected to one and same surface of the first lead.
18. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having on one main surface thereof a first bonding pad (inherit) and a second bonding pad (nherit) both disposed along one side of the one main surface; a second semiconductor chip **12b** quadrangular in shape and having on one main surface thereof a third bonding pad (inherit) and two fourth bonding pads (inherit) interconnected electrically, the third and fourth bonding pads being disposed along one side of the one main surface of the second semiconductor chip, the third bonding pad being disposed between the fourth bonding pads, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip in such a manner that the one side of the one main surface thereof is opposite to the one side of the one main surface of the first semiconductor chip; a first lead **11** and a second lead **11** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the one side of the first semiconductor chip; a first bonding wire **14a** for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead; a second bonding wire **14a** for connecting the second bonding pad on the first semiconductor chip with the inner lead portion of the second lead; a third bonding wire **14b** for connecting the third bonding pad on the second semiconductor chip with the inner lead portion of the first lead; a fourth bonding wire **14b** for connecting one of the two fourth bonding pads on the second semiconductor chip with the inner lead portion of the second lead; and a resin seal member for sealing the first and second semiconductor chips, the inner lead portions of the first and second leads, and the first, second, third and fourth bonding wires.
19. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** which is quadrangular and which has a first bonding pad (inherit) on one side of one main surface thereof; a second semiconductor chip **12b** which is quadrangular and which has a second bonding pad (inherit) on one side of one main surface thereof, the one side of the one main surface of the second

semiconductor chip being disposed on the one main surface of the first semiconductor chip in an opposed relation to the one side of the one main surface of the first semiconductor chip; a lead **11** having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the one side of the first semiconductor chip; a first bonding wire **14a** connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the lead; a second bonding wire **14b** for connecting the second bonding pad on the second semiconductor chip with the inner lead portion of the lead; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portion of the lead, and the first and second bonding wires, wherein the second semiconductor chip is disposed on the one main surface of the first semiconductor chip in a state such that a central point of the second semiconductor chip is displaced so as to be positioned on one side of the first semiconductor chip with respect to a central point of the first semiconductor chip.

20. A semiconductor device according to claim 19, Choi et al. show wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the first semiconductor chip and a second center line orthogonal to the first center line, and wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the one side of the second semiconductor chip and a second center line orthogonal to the first center line.

21. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** which is quadrangular in plan and which has a first bonding pad (inherit) on a first side of one main surface thereof and a second bonding pad (inherit) on a second side of the one main surface contiguous to the first side; a second semiconductor chip **12b** which is quadrangular in plan and which has a third bonding pad (inherit) on one side of one main surface thereof and a fourth bonding pad (inherit) on a second side of the one main surface contiguous to the first side; the second semiconductor chip being disposed on the one main surface of the first semiconductor chip in a state such that the first side of the one main surface thereof is opposed to the first side of the first semiconductor chip and the second side of the one main surface thereof is opposed to the second side of the first semiconductor chip; a first lead **11** having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed outside the first side of the first

semiconductor chip; a second lead **11** having an inner lead portion and an outer lead potion integral with the inner lead portion, the inner lead portion being disposed outside the second side of the first semiconductor chip; a first bonding wire **14a** for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the first lead; a second bonding wire **14b** for connecting the first bonding pad on the second semiconductor chip with the inner lead of the first lead; a third bonding wire **14a** for connecting the second bonding pad on the first semiconductor chip with the inner lead of the second lead; a fourth bonding wire **14b** for connecting the second bonding pad on the second semiconductor chip with the inner lead of the second lead; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portions of the first and second leads, and the first to fourth bonding wires, wherein the second semiconductor chip disposed on the one main surface of the first semiconductor chip in a state such that a central point thereof is displaced so as to be positioned on the first and second sides of the first semiconductor chip.

22. A semiconductor device according to claim 21, Chio et al. show wherein the central point of the first semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the first semiconductor chip and a second center line orthogonal to the first center line, and wherein the central point of the second semiconductor chip is a point of intersection of a first center line extending in the same direction as the first side of the second semiconductor chip and a second center line orthogonal to the first center line.

23. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device comprising: a first semiconductor chip **12a** which is quadrangular and which has a first bonding pad (inherit) on one side of one main surface thereof; a second semiconductor chip **12b** which is quadrangular and which has a second bonding pad (inherit) on one side of one main surface thereof, the second semiconductor chip being disposed on the one main surface of the first semiconductor chip; a lead **11** having an inner lead and an outer lead integral with the inner lead, the inner lead being disposed outside the one side of the first semiconductor chip; a first bonding wire **14a** for connecting the first bonding pad on the first semiconductor chip with the inner lead portion of the lead; a second bonding wire **14b** for connecting the second bonding pad on the second semiconductor chip with the inner lead portion of the lead; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portion of the lead, and the first and second bonding wires, wherein the second semiconductor chip is

disposed on the first semiconductor chip in a state such that one side of the second semiconductor chip is opposed to two sides contiguous to each other of the first semiconductor chip so as to shorten the length of the second bonding wire.

24. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads (inherit) being formed on the first main surface; a second semiconductor chip **12b** having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads (inherit) being formed on the first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip; a plurality of leads each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of bonding wires **14a,14b** for connecting the plural bonding pads on the first and second semiconductor chips with the inner lead portions of the plural leads respectively; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portions of the plural leads, and the plural bonding wires, wherein the second semiconductor chip is smaller in thickness than the first semiconductor chip.

25. A semiconductor device according to claim 24, Choi et al. show wherein the second semiconductor chip is bonded to the first main surface of the first semiconductor chip through an adhesive layer.

26. A semiconductor device according to claim 25, Choi et al. show wherein the adhesive layer is formed by a bonding resin film.

27. A semiconductor device according to claim 25, Choi et al. show wherein the distance from the first main surface of the first semiconductor chip to the second main surface of the second semiconductor chip is smaller than the thickness of the first semiconductor chip.

28. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having a first main surface and a second main surface opposed to each other, with a plurality of bonding pads (inherit) being formed on the first main surface; a second semiconductor chip **12b** having a first main surface and a second main surface opposed to each other, with a plurality of bonding

pads (inherit) being formed on the first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip; a plurality of leads **11** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of bonding wires**14a,14b** for connecting the plural bonding pads on the first and second semiconductor chips with the inner lead portions of the plural leads respectively; and a resin sea! member **15** for sealing the first and second semiconductor chips, the inner lead portions of plural leads, and the plural bonding wires, wherein the bonding pads on the second semiconductor chip are larger in plane size than the bonding pads on the first semiconductor chip.

29. Choi et al. (figures 1 to 7) specifically figure 1 show a semiconductor device **10** comprising: a first semiconductor chip **12a** having a first main surface and a second main surface opposed to each other, with a plurality of quadrangular bonding pads (inherit) being formed on the first main surface; a second semiconductor chip **12b** having a first main surface and a second main surface opposed to each other, with a plurality of quadrangular bonding pads (inherit) being formed on the first main surface, the second semiconductor chip being disposed on the first semiconductor chip in a state such that the second main surface thereof is opposed to the first main surface of the first semiconductor chip, the second semiconductor chip being smaller in plane size than the first semiconductor chip; a plurality of leads **11** each having an inner lead portion and an outer lead portion integral with the inner lead portion, the inner lead portion being disposed at a position around the first semiconductor chip; a plurality of first bonding wires **14a** for connecting the plural bonding pads on the first semiconductor chip with the inner lead portions of the plural leads respectively; a plurality of second bonding wires **14b** for connecting the plural bonding pads on the second semiconductor chip with the inner lead portions of the plural leads respectively; and a resin seal member **15** for sealing the first and second semiconductor chips, the inner lead portions of the plural leads, and the first and second bonding wires, wherein the bonding pads on the second semiconductor chip are each formed in a rectangular shape wherein a side located in an extending direction of the bonding wires is longer than a side opposed to the leads.

30. A semiconductor device according to claim 29, Choi et al. show wherein the bonding pads on the second semiconductor chip are larger in plane size than the bonding pads on the first semiconductor chip.
31. A semiconductor device according to claim 29, Choi et al. show wherein the second bonding wires each have a first portion extending in a direction perpendicular to the first main surface of the second semiconductor chip and a second portion extending along the first main surface of the second semiconductor chip, and wherein the first portion is positioned above the inner lead portions.

The listed references are cited as of interest to this application, but not applied at this time.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/723-25,728,777,784,786,666,676,685,686,692,<br>696,698,796,777,684 | 11/25/02 |
| Other Documentation:<br>foreign patents and literature in 257/723-<br>25,728,777,784,786,666,676,685,686,692,<br>696,698,796,777,684 | 11/25/02 |
| Electronic data base(s):<br>U.S. Patents EAST | 11/25/02 |

***Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.***

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

11/26/02

Primary Examiner
Alexander O. Williams